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Processors Speed Acceleration Models Based on Single and Multi-Core Computing

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Abstract the power and energy normalisation to increase the performance of muti-core processors is one of the challenges for processors designers. Several models cover the power and performance of multi-core processors. In this work, we will try to explain such models and proposing an excellent model that concerns the advantages and drawbacks of these architecture models. The target is to get a high acceleration based on the optimum balance between power and performance. This is achieved by including additional process's features. For multi-core processors using the pipelining techniques show a very high acceleration but with low power and energy normalisation. Working sequentially and concentrating on the multi- core principle show an adequate speed acceleration with high normalised power and energy. The results show better performance using the extended model between 0.08% to 0.15%.

***Index Terms*— multi-core processors; processor' acceleration; energy saving; power and energy normalization.**

I. INTRODUCTION

THe possible approaches to accelerate the sequential part is to enhance the frequency of the multi- core for the sequential part. For example, Intel Turbo Boost technology enables transient overclocking for a dedicated core if the other cores are in an idle state [3]. The reasonable technique since only one core is used for the sequential part. However, the method inevitably causes increased energy consumption due to the increased operating frequency. An optimum balance should be performed between performance and energy should be carefully considered. Presenting here a performance and power model and show the energy efficiency through the proposed modelling method. [1].

The market keeps the cost and performance f the multi-core processors on the top of their concerns. Intel founder predicted (based on Moore's Law [4]) that the number of transistors would be very high and on them, the processor's speed will be depended. On the other hand, the complexity will be increased by increasing the performance of the microprocessor [5].

Multi-core processors contain several cores on one chip [5]. The parallel principle process is the main idea behind enhancing the performance of the microprocessor using multi-core architecture [6].

Several Laws can represent the performance of multi-core processors. For example, the prediction of processor's performance based on the concept of Base Core Equivalent (BCE) resource to predict the performance based on processor design styles [7].

Sun and Chen analysed this feature using more promised model to enhance the processor's speed based on the scalability than on the processor's design.

In [8], the Deeper Pipelines are implemented to increase the performance of the microprocessors. This approach did not consider the hardware reconstruction and therefore the power and energy consumption increase. Th multi-core as parallel processing techniques and using pipelining will increase the processing speed, but the power consumption will be increased nad the heating problem in the multi-core processes will be on of the biggest issue that needs a powerful cooling process.

Modern embedded systems execute multiple operations, both sequentially and concurrently. These applications are

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experimented on different platforms generating varying power consumption and system workloads (CPU or memory intensive or both). As a result, determining the most energy-efficient system configuration (i.e. the number of parallel threads, their core allocations and operating frequencies) tailored for each kind of workload and application scenario is extremely challenging [10]. In [10], the model normalised power performance (regarding IPS/Watt) underpinning analytical power and performance models, derived through multivariate linear regression (MLR).

To explain the main Idea, we will have a background about the main power and energy models.

II. DYNAMIC VOLTAGE FREQUENCY SCALING (DVFS)

Dynamic voltage and frequency scaling (DVFS) is a technique to save power on a broad range of computing systems[11].

DVFS is used to decrease the power consumption of CMOS integrated circuit such as a modern computer microprocessor. Based on the frequency,

$$P = CfV^2 + P_{static} \quad (1)$$

where C is the transistor's capacitance, f is the operating frequency, and V is the voltage supplied the processor. The voltage needed for stability of the operation can be defined by the frequency at which the circuit was clocked, and can be reduced if the frequency is also reduced. This can yield a significant reduction in power consumption because of the V^2 relationship is shown above [11].

In [12], The Authors analysed and examined the potential of DVFS across three platforms with the current generation of AMD processors in various aspects viz. Scaling of Silicon Transistor technology, Improved memory performance, Improved sleep/ idle mode, Multicore Processors.

The results show that on the most current platform, the effectiveness of DVFS is clearly decreased, and actual savings are only observed when short executions are implemented (at a higher frequency) are padded with the energy consumed when idle.

In [11], analysed the best-case effectiveness of DVFS on three recent generations of AMD Opteron processors, using a memory-bound benchmark.

Results in [11] show that on the most current platform, the effectiveness of DVFS is clearly decreased, and real savings are only observed when executions are made shorter (at higher frequencies). The analysis is made simple through considering a single memory-bound processor. However, this is the only case where DVFS has the highest chance of being effective. DVFS is still effective with other platforms. Power consumption and reduced dynamic power range. Given the shrinking potential for decreasing the energy consumption, only a time is needed for manufacturers until abandon DVFS in favour of ultra low-power sleep modes.

III. GUSTAFSON'S MODEL AND AMDAHL'S LAW

Gustafson's Law can be written as the following way:

$$S_{latency}(s) = 1 - p + sp \quad (2)$$

where

$S_{latency}$ is the theoretical speedup; S is the speedup of the implementation of the part of the task that benefits from the improvement of the resources of the system;

$\boldsymbol{p}$ is the percentage of the execution workload of the whole task concerning the part that benefits from the enhancement of the resources of the system before the improvement.

Gustafson's law addresses the shortcomings of Amdahl's law, which is based on the assumption of a fixed problem size, that is an execution workload that does not change on the performance improvement of different resources. Gustafson's law instead proposes that programmers tend to set the size of problems to fully exploit the computing power that becomes available as the resources improve. Therefore, if the faster equipment is available, larger problems can be solved within the same time.

The impact of Gustafson's Law was to shift[citation needed] research goals to select or reformulate problems so that solving a larger problem in the same amount of time would be possible. In a way, the Law redefines efficiency, due to the possibility that limitations imposed by the sequential part of a program may be countered by increasing the total amount of computation.

Amdahl's Law reveals a limitation in, for example, the ability of multiple cores to reduce the time it takes for a computer to boot to its operating system and be ready for use. Assuming the boot process was mostly parallel, quadrupling computing power on a system that took one minute to might reduce the boot time to just over fifteen seconds. However, greater and greater parallelization would eventually fail to make bootup go any faster if any part of the boot process were inherently sequential.

Gustafson's Law argues that a fourfold increase in computing power would instead lead to a similar increase in expectations of what the system will be capable of. If the one-minute load time is acceptable to most users, then that is a starting point from which to increase the features and

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functions of the system. The time taken to boot to the operating system will be the same, i.e. one minute, but the new system would include more graphical or user-friendly features.

The Amdahl's law can be written as:

$$SP(N) = \frac{T'(1)}{T(1)} = \frac{1}{(1-p) + \frac{p}{N}} \quad (3)$$

From the relation of scaled and unscaled execution time the following equation for speedup can be calculated [13]:

$$SP(N) = \frac{T'(1)}{T(1)} = (1-p) + pN \quad (4)$$

comparing (2) and (3), show that they are similar where N is the number of cores and SP is the speedup as a function of N.

Sun and Ni mixed the previous two speedup models by considering the memory bounded constraints [14], [15]. In this model the execution time and the workload change according to the memory capability. The parameter g (N) reflects the scaling of the workload about scaling the memory with the number of cores:

$$SP(N) = \frac{T'(1)}{T(N)} = \frac{(1-p) + p.{}_g(N)}{(1-p) + \frac{P.{}_g(N)}{N}} \quad (5)$$

IV. PROPOSED SPEED ACCELERATION MODELS

Models in (3), (4) and (5) are well-known as speed acceleration models. Our proposed model is an extended Sun and Ni model due to its mixed characters of the other two models.

The extended model can be expressed as in equation (6) [13].

$$SP(N) = \frac{T'(1)}{T(N)} = \frac{(1-p) + p.{}_g(\overline{N})}{\frac{(1-p)}{\alpha x} + \frac{P.{}_g(\overline{N})}{N_\alpha}} \quad (6)$$

N_α is called a performance-equivalent number of BCEs. In other words, this performance is equal to N_α BCE cores executing the same parallel code; Performance-wise, the presented models describe heterogeneity using the following normal form representation. A considered heterogeneous system consists of X clusters (types) of homogeneous cores with some cores defined as a vector $N_\alpha = (N_1, \ldots, N_X)$. Vector $\alpha = (\alpha_1, \ldots, \alpha_X)$ defines the performance of each core by cluster (type) in relation to some base core equivalent (BCE), such that for all $1 \le i \le X$ we have $IPS_i = \alpha_i \cdot IPS_1$.

V. EXPERIMENTAL RESULTS

Multi-core performance: experiments in this section are run with both A7 and A15 cores at 1500MHz. In this work, we set BCE to A7. Hence αA7 = 1; and αA15 can be found as a ratio of execution times αA15 = TA7/TA15, as shown in Table II. It can be seen that A15 is expectedly faster than A7 for integer arithmetic and logarithm calculation, however, square root calculation is faster on A7. This is confirmed multiple times in many experiments. Three different benchmarks provide different αA15 values, which strengthens our study. For sqrt bench

bench (Sqrt)				Speedup		
	NA7	NA15	Times ms	Normal Model	Exyended Model	(%)
0.3	3	0	59992	1.2505	1.40056	0.12
0.3	0	4	61911	1.2117	1.369221	0.13
0.3	2	2	61910	1.2118	1.39357	0.15
0.3	3	4	59359	1.2638	1.402818	0.11
0.9	3	0	29988	2.5017	2.901972	0.16
0.9	0	4	25977	2.8879	3.147811	0.09
0.9	2	2	25961	2.8897	3.120876	0.08
0.9	3	4	18300	4.0995	4.59144	0.12

The results show better performance using the extended model between 0.08% to 0.15%.

VI. CONCLUSIONS

The power and energy normalisation to increase the performance of muti-core processors is one of the challenges for processors designers. Several models cover the power and performance of multi-core processors. In this work, we will try to explain such models and proposing an excellent model that concerns the advantages and drawbacks of these architecture models. The target is to get a high acceleration based on the optimum balance between power and performance. This is achieved by including additional process's features. For multi-core processors using the pipelining techniques show a very high acceleration but with low power and energy normalisation. Woking sequentially and concentrating on the multi- core principle show an adequate speed acceleration with high normalised power and energy.

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